coupled and associated to ones of the plurality of functional units;

partitioning the register file segments into global registers and local registers;

operating the plurality of functional units;

accessing the global registers by the plurality of functional units; and

accessing the local registers by the functional unit associated with the register file segment containing the local registers.

REMARKS

Claims 1-29 are pending in the above-identified application. Claims 23-29 are rejected under 35 U.S.C. §112, second paragraph; Claims 1-29 are rejected under 35 U.S.C. §103(a); and Claims 1-29 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 09/204,479 in view of Yung (U.S. 5,592,679). The rejections are respectfully traversed in light of the following remarks, and reconsideration is requested.

A telephonic interview was held on March 2, 2001, between the Examiner, Matthew Spark and Ken Koestner. During the interview, with respect to the rejection of Claim 1, the Examiner stated that he did not believe the structural differences between the references and Claim 1 matters as he believed the references and Claim 1 were equivalent and, in his words, "functionally identical." The Examiner expressed similar comments with respect to Claim 15. When asked, the Examiner repeated his assertion that the structural differences between the references and the claims did not matter as he believed the claims and references to be functionally identical. The Examiner failed to assert any case law or MPEP section to support this unique theory that claimed structure is irrelevant in determining patentability.

Claims 23-29 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In a prior Office Action, the Examiner stated:

> The method as recited is merely a flow chart of an idea to operate a processor. The steps as recited in the claim combination are not actually performed by the processors such that a meaningful result is achieved. The method steps actually are reciting the architectural structure (see the first four steps of claim 23) of a processor and the functions (see the last two steps of claim 23) of the components thereof.

In response, Applicants respectfully contends that the above rejection is improper under MPEP2173.05(v). MPEP2173.05(v) [Mere Function of Machine] states:

> In view of the decision of the Court of Customs and Patent Appeals in *In re Tarczy-Hornoch*, 39 F.2d 856, 158 USPQ 141 (CCPA 1968), process or method claims are not subject to rejection by Patent and Trademark Office examiners under 35 USC 112, second paragraph, solely on the ground that they define the inherent function of a disclosed machine or apparatus. The court in re Tarczy-Hornoch held that a process claim, otherwise patentable, should not be rejected merely because the application of which it is part discloses apparatus which will inherently carry out the recited steps.

Claims 23-29 state:

> 23. A method of operating a processor comprising:
> operating a plurality of functional units; and
> dividing a register file into a plurality of register file segments;
> coupling and associating ones of the plurality of register file segments with ones of the plurality of functional units;
> partitioning the register file segments into global registers and local registers;
> accessing the global registers by the plurality of functional units;
> accessing the local registers by the functional unit associated with the register file segment containing the local registers.
> 24. A method according to Claim 23 further comprising:
> addressing the local registers and global registers using register addresses in an address space that is defined for a register file segment/ functional unit pair.
> 25. A method according to Claim 23 further comprising:
> addressing the local registers in a register file segment using register

addresses in a local register range outside the global register range that are assigned within a single register file segment/ functional unit pair.

26. A method according to Claim 23 further comprising:
addressing the local register range the same for the plurality of register file segment/ functional unit pairs and address registers locally within a register file segment/ functional unit pair.

27. A method according to Claim 23 further comprising:
including N physical registers in the register file;
duplicated the physical registers into M register file segments, the register file segments having a reduced number of read and/or write ports in comparison to a nonduplicated register file, but each having the same number of physical registers.

28. A method according to Claim 27 further comprising:
partitioning the register file segments into NG global and NL local register files where NG plus NL is equal to N;
operating the register file equivalently to a register file having NG + (M * NL) total registers available for the M functional units, the number of address bits for addressing the NG + (M * NL) total registers being equal to the number of bits B that are used to address N = 2B registers; and
addressing the local registers for ones of the M register file segments using the same B-bit values.

29. A method according to Claim 27 further comprising:
programmably partitioning the register file so that the number NG of global registers and number NL of local registers is selectable and variable.

The above claims clearly fall within the rubric of MPEP2173.05(v) in that method claims are not subject to rejection solely on the ground that they define the inherent function of the disclosed apparatus.

The Examiner contends that

> none of the steps as recited in the rejected claims are inherent function of a machine or apparatus.

However, the Examiner specifically admits that method actually recites the architectural structure (see the first four steps of claim 23) of a processor and the functions (see the last two steps of claim 23) of the components thereof. It is contradictory for the Examiner to admit to the functions performed by the structures and then claim that those functions are not inherent. Therefore, for the above reasons, and in light of the amendments

to Claim 23, Applicant respectfully requests reconsideration and withdrawal of the rejections of Claims 23-29 under 35 U.S.C. § 112, second paragraph.

Claims 1-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Yung (U.S. 5,592,679) in view of Nishimoto (U.S. 6,023,757). In the rejection, the Examiner stated:

> Applicants contended that there is no mention in Yung that a plurality of processors share a single global register file. Figures 1 and 2 in Yung clearly show a plurality of functional (execution) units (processing elements or processors).
>
> Applicants further contended that there is no mention in Yung that a register file is implemented in a manner as recited in claim 1. The recitation of the register file merely consists of functional languages. There are no circuits recited for implementing the register as reicted [sic] in lines 3-9 of claim 1.
>
> Applicants appear to contend on page 5 of the remarks that applicants disclose a central register file. It is not clear what applicants meant by that. Claim 1 clearly recites a register file, similar to Yung's, being partitioned into segments (not central).
>
> With respect to the remarks on pages 5-7, it appears that applicants compare their disclosure with the disclosure of Yung rather than the claimed invention with the teaching of Yung as applied by the Examiner. The Yung reference meets all the claimed structural limitations. Applicants are unable to identify one single claimed component that is not in Yung.
>
> Applications [sic] further contended that there is no teaching to combine the two references. The court held that (see B.F. Goodrich Co. v. Aircraft Braking Systems Corp., 72 F.3d 1577, 1583, 37 USPQ2d 1314, 1319 (Fed. Cir. 1996) and In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988)) while there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination. Rather, the test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art. See In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991) and In re Keller, 642 F.2d 413, 425, 208 USPQ2d 871, 881 (CCPA 1981). More over, in evaluating such references it is proper to take into account not only the specific teachings of the references but also the inference which one skilled in the art would reasonably be expected to draw therefrom. In re Preda, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968).

In response, Applicants respectfully contend that not only do the combined references fail to show the features of the claimed invention but the obviousness rejection under 35 U.S.C. § 103 cannot be established by combining the teachings of Yung and Nishimoto because there is no suggestion or motivation in the cited references for combining Yung and Nishimoto. The Examiner mistakenly believes that Applicants compare their disclosure with the disclosure of Yung rather than the claimed invention. The Applicants submit that the teachings of Yung do not read on the claims of the instant application, as applied by the Examiner.

The Examiner clearly misconstrues Claim 1. A register file is divided into a plurality of register file segments. Each register file segment is partitioned into a global register and a local register. It is a structure that Yung does not disclose!

The Examiner fails to provide any explanation as to WHY the cited references are combinable. The Examiner is apparently using hindsight. As admitted by the Examiner, Yung does not have a decoder! Although Nishimoto has a decoder for processing VLIW, the Examiner fails to explain what the "clear and particular " teaching of Nishimoto is that allows one of ordinary skill to conclude that the references are combinable. The Examiner merely seems to fill in the gap by saying because VLIW and decoders are well-known in the art, and that somehow one of ordinary skill in the art would automatically think decoder and VLIW when looking at Yung. What suggests adding a decoder and VLIW to Yung? The Examiner fails to provide any support or explanation for this necessary component of a prima facie obviousness rejection.

The Applicant claims register file segments where each segment is broken into local and global registers. Yung teaches separate individual local register files and a shared global register file but not contained in a single register file segment as is claimed by Applicant.

The Examiner misconstrues what is required to combine references for a prima facie case of obviousness. In Ruiz v A.B. Chance Co., 234 F.3d 654 (Fed. Cir. 2000), the Court specifically held *specific findings must be made establishing why it was "apparent" to use a feature of found in one reference in the context with what is disclosed in another reference.* (The district court must make specific findings establishing why it was "apparent" to use the screw anchor of the Fuller and Rupiper method in combination with the metal bracket as used in the Gregory patents.).

While the references need not expressly teach that the disclosure contained therein should be combined with another, see Motorola, Inc. v. Interdigital Tech. Corp., 121 F.3d 1461, 1472, 43 USPQ2d 1481, 1489 (Fed. Cir. 1997), the showing of combinability must be "clear and particular." In re Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617. [Emphasis added]

The Examiner has failed to make any showing of combinability that is "clear and particular". Yung discloses a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor. (Yung, Abstract, col. 2, lines 65-67). However, there is no mention that a register file is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers, as is being claimed by Applicant.

Furthermore, Yung teaches a different method from Applicant in that Yung teaches a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor. (Yung, Abstract, col. 2, lines 65-67). Yung teaches away from the claimed invention in that Yung states that "[a] single centralized register file is not

ideal because interconnecting the large fast global memory to a large number of execution units is prohibitively expansive in silicon area and requires extremely complex circuitry with many I/O ports." The claimed invention includes a single centralized register file. Yung is classified in class 712, subclass 23. Therefore, Yung is directed to solving the problem of a superscalar processor in that it is "subject matter comprising an architecture which determines a group of upcoming instructions which do not mutually interfere with each other and issue or dispatches this group simultaneously" (See Class Definitions, Class 712, Subclass 23). Thus, Yung teaches a multi-level instruction scheduling system for controlling multiple execution pipes of a distributed data flow processor (Yung, Abstract, col. 2, lines 65-67) while Applicant teaches storage having local and global access regions for subinstructions in a Very Long Instruction Word (VLIW) processor (Specification, page 1, lines 7-8).

As admitted by the Examiner, Yung does not teach the use of a decoder for decoding VLIW nor does it teach a processor having a plurality of functional units including a multi-ported register file that is divided into a plurality of separate register file segments, each of the register file segments being associated to one of the plurality of functional units where the register file segments are partitioned into local registers and global registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers.

On the other hand, while the invention disclosed in Nishimoto relates generally to a microprocessor or microcomputer (col. 1, lines 4-5) and specifically to a method and apparatus for use in a data processor to cause the data processor to attain high-speed performance while maintaining software compatibility (col. 1, lines 5-9), Nishimoto is directed to addressing a completely different problem than Yung. Yung was addressed to solving the problem of a multi-level instruction scheduling system for controlling multiple

execution pipes of a distributed data flow processor. (Yung, Abstract, col. 2, lines 65-67). Nishimoto, on the other hand, discloses a method for causing a data processor to attain high-speed performance while maintaining software compatability (col. 1, lines 5-9). There is no suggestion in Yung that a processor include a plurality of functional units; and a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers, is desirable nor does Nishimoto suggest a combination of its joint processing technique with the instruction grouping and dispatching technique of Yung. Nishimoto is classified in class 712, subclass 209. Therefore, Yung is directed to solving the problem of decoding instructions to accommodate plural instruction interpretations (See Class Definitions, Class 712, Subclass 209) while Applicant teaches storage having local and global access regions for subinstructions in a Very Long Instruction Word (VLIW) processor (Specification, page 1, lines 7-8). The claimed invention teaches a processor including a plurality of functional units; and a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers. Neither Yung, Nishimoto nor the references combined teach the claimed invention.

Obviousness is tested by "what the combined teachings of the references would have suggested to those of ordinary skill in the art." In re Keller, 642 F.2d 413, 425, 208 USPQ

871, 881 (CCPA 1981). But obviousness "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." ACS Hosp. Sys. Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). Thus, "teachings of references can be combined only if there is some suggestion or incentive to do so." Id. Applicants, thereby, contend that there is no suggestion or incentive to combine Yung and Nishimoto because Yung and Nishimoto are directed to solving different problems with different solutions, as outlined above.

Thus, for a obviousness combination, the "critical inquiry is whether 'there is something in the prior art as a whole to suggest the desirability, and thus the obviousness of making the combination.'" Fromson v. Advance Offset Place, Inc., 755 F.2d 1549, 1556, 225 USPQ 26, 31 (Fed. Cir. 1985) *quoting* Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1453, 1452, 221 USPQ 481, 488 (Fed. Cir. 1984). In other words, the "mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." In re Gordon, 773 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) *citing* Carl Schenck, A.G. v. Nortron Corp., 713 F.2d 782, 787, 218 USPQ 698, 702 (Fed. Cir. 1983). Yung does not suggest the desirability of a combination with Nishimoto because, as mentioned above, Yung and Nishimoto are directed toward different problems with different solutions. Accordingly, Yung does not suggest to one skilled in the art the desirability to search for other ways that improve storage such that the storage has local and global access regions for subinstructions in a Very Long Instruction Word (VLIW) processor, much less for a combination with a reference having a different problem and different solution, such as Nishimoto.

Furthermore, the "statute, §103, requires much more, i.e., that it would have been obvious to produce the claimed invention at the time it was made without the benefit of

hindsight." Orthokinetics, Inc. v. Safety Travel, Chairs, Inc., 806 F.2d 1565, 1575, 1 USPQ2d 1081, 1087 (Fed. Cir. 1986). "When prior art references require selective combination by the court to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself." Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985) *citing* ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577 & n.14, 221 USPQ 929, 933 & n.14 (Fed. Cir. 1984). Applicants believe the motivation to combine Yung with Nishimoto is derived from Applicants' invention since there is no suggestion in the cited references for the desirability of such a combination. The instant application is directed to a processor including a plurality of functional units; and a register file that is divided into a plurality of register file segments, ones of the plurality of register file segments being coupled to and associated with ones of the plurality of functional units, the register file segments being partitioned into global registers and local registers, the global registers that are accessible by the plurality of functional units, the local registers being accessible by the functional unit associated with the register file segment containing the local registers.

Therefore, because Applicants contend that the combination of Yung and Nishimoto was both substantively and procedurally improper, Applicants respectfully request reconsideration and withdrawal of the rejections to Claims 1-29 under 35 U.S.C. § 103(a).

Claims 1-29 were provisionally rejected under the judicially created doctrine of double patenting over claim 1-22 of copending Application No. 09/204,479 in view of Yung (U.S. 5,592,679). In a Prior Office action, the Examiner stated:

> The claims of copending applications recite a system having a plurality of functional units and a register file. The copending claims do not specify whether the registers are of global and local type. Yung teaches both types of registers. It would have been obvious to a person of ordinary skill in the art to incorporate a global register in the system of copending application such that the processors are able to share

information via global registers.

This is a provisional obviousness-type double patenting rejection.

Applicants recognize the provisional nature of the rejections, and will address the substantive aspect of this issue in future communications to this Office should Claims 1-22 of copending Application No. 09/204,479 be allowed at some future point in time and in the same, or substantially the same, form as they now presently exist.

CONCLUSION

For the foregoing reasons, Applicant believes the pending Claims 1-29 are allowable, and a Notice of Allowance is respectfully requested. The Examiner is invited to call the Applicants' Attorney at (949) 718-6780 for any questions with this response.

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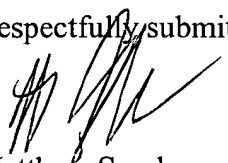
Respectfully submitted,



Matthew Spark
Attorney for Applicant(s)
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ATTACHMENT A

This response amends Claim 23 as follows:

23. A method of operating a processor comprising:

providing a processor including a plurality of functional units;

[operating a plurality of functional units; and]

[dividing] a register file divided into a plurality of register file segments [;] , the plurality of register file segments being

[coupling] coupled and [associating] associated to ones of the [plurality of register file segments with ones of the] plurality of functional units;

partitioning the register file segments into global registers and local registers;

operating the plurality of functional units;

accessing the global registers by the plurality of functional units; and

accessing the local registers by the functional unit associated with the register file segment containing the local registers.